

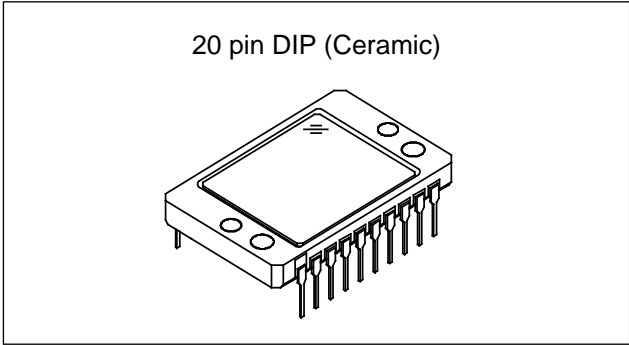
2/3-inch CCD Image Sensor for EIA Black-and-White Video Cameras

Description

The ICX082AL is an interline CCD solid-state image sensor suitable for EIA black-and-white video cameras with a 2/3-inch optical system.

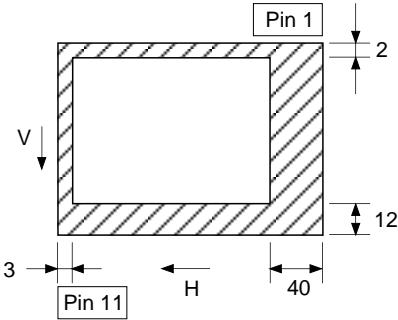
High sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field period readout system and an electronic shutter with variable charge-storage time.



Features

- High sensitivity (+6dB compared with the ICX022BL)
- Low smear (-20dB compared with the ICX022BL)
- High resolution, Low dark current
- Excellent antiblooming characteristics
- Continuous variable-speed shutter



Optical black position
(Top View)

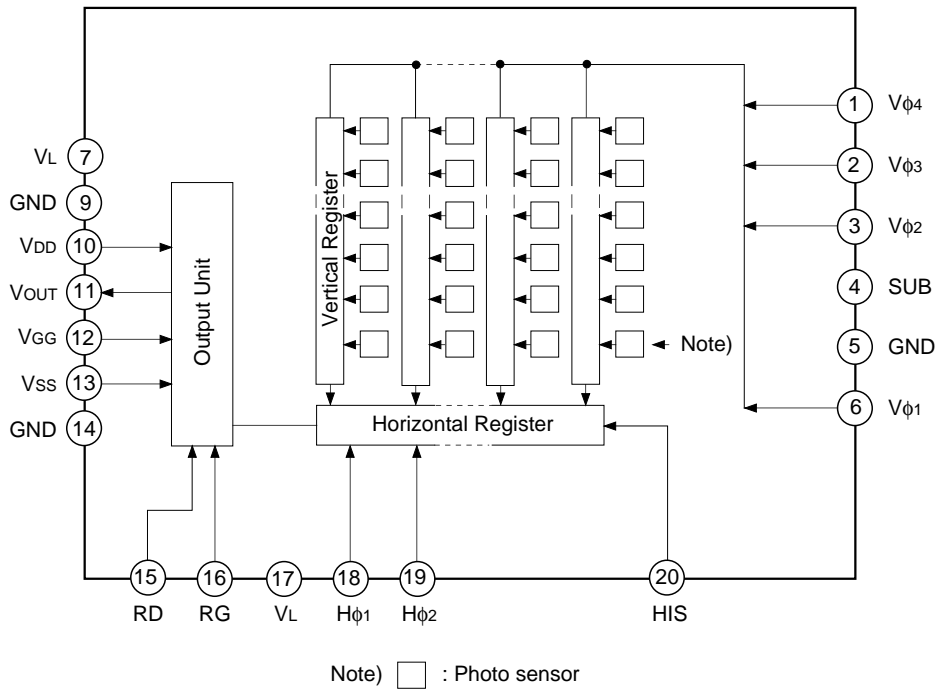
Device Structure

- Interline CCD image sensor
- Optical size: 2/3-inch format
- Number of effective pixels: 768 (H) × 494 (V) approx. 380K pixels
- Total number of pixels: 811 (H) × 508 (V) approx. 410K pixels
- Chip size: 10.25mm (H) × 8.5mm (V)
- Unit cell size: 11.6μm (H) × 13.5μm (V)
- Optical black:
 - Horizontal (H) direction: Front 3 pixels, rear 40 pixels
 - Vertical (V) direction: Front 12 pixels, rear 2 pixels
- Number of dummy bits:
 - Horizontal 22
 - Vertical 1 (even fields only)
- Substrate material: Silicon

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram and Pin Configuration

(Top View)



Pin Description

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---------|-----------------|----------------------------------|---------|------------------|---------------------------------------|
| 1 | V ϕ 4 | Vertical register transfer clock | 11 | V _{OUT} | Signal output |
| 2 | V ϕ 3 | Vertical register transfer clock | 12 | V _{GG} | Output amplifier gate bias |
| 3 | V ϕ 2 | Vertical register transfer clock | 13 | V _{SS} | Output amplifier source |
| 4 | SUB | Substrate (overflow drain) | 14 | GND | GND |
| 5 | GND | GND | 15 | RD | Reset drain |
| 6 | V ϕ 1 | Vertical register transfer clock | 16 | RG | Reset gate clock |
| 7 | V _L | Protective transistor bias | 17 | V _L | Protective transistor bias |
| 8 | NC | | 18 | H ϕ 1 | Horizontal register transfer clock |
| 9 | GND | GND | 19 | H ϕ 2 | Horizontal register transfer clock |
| 10 | V _{DD} | Output amplifier drain power | 20 | HIS | Horizontal register input source bias |

Absolute Maximum Ratings

| Item | | Ratings | Unit | Remarks |
|----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|-------------|------|---------|
| Substrate voltage SUB – GND | | –0.3 to +55 | V | |
| Supply voltage | HIS, V _{DD} , RD, V _{OUT} , V _{SS} – GND | –0.3 to +20 | V | |
| | HIS, V _{DD} , RD, V _{OUT} , V _{SS} – SUB | –55 to +10 | V | |
| Vertical clock input voltage | Vertical clock input pins – GND | –15 to +20 | V | |
| | Vertical clock input pins – SUB | to +10 | V | |
| Voltage difference between vertical clock input pins | | to +15 | V | *1 |
| Voltage difference between horizontal clock input pins | | to +17 | V | |
| H ϕ ₁ , H ϕ ₂ – V ϕ ₄ | | –17 to +17 | V | |
| H ϕ ₁ , H ϕ ₂ , RG, V _{GG} – GND | | –10 to +15 | V | |
| H ϕ ₁ , H ϕ ₂ , RG, V _{GG} – SUB | | –55 to +10 | V | |
| V _L – SUB | | –65 to +0.3 | V | |
| V ϕ ₁ , V ϕ ₃ , HIS, V _{DD} , RD, V _{OUT} – V _L | | –0.3 to +30 | V | |
| RG – V _L | | –0.3 to +24 | V | |
| V ϕ ₂ , V ϕ ₄ , V _{GG} , V _{SS} , H ϕ ₁ , H ϕ ₂ – V _L | | –0.3 to +20 | V | |
| Storage temperature | | –30 to +80 | °C | |
| Operating temperature | | –10 to +60 | °C | |

*1 +27V (Max.) when clock width < 10 μ s, clock duty factor < 0.1%.

Bias Conditions

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|-----------------------------------------------|---------------------------|-------------------------------------|-------|------|------|------------------------------------|
| Output amplifier drain voltage | V _{DD} | 14.7 | 15.0 | 15.3 | V | |
| Reset drain voltage | V _{RD} | 14.7 | 15.0 | 15.3 | V | V _{RD} = V _{DD} |
| Output amplifier gate voltage | V _{GG} | 3.8 | 4.2 | 4.6 | V | |
| Output amplifier source | V _{SS} | Grounded with 750 Ω resistor | | | | \pm 5% |
| Substrate voltage adjustment range | V _{SUB} | 9 | | 19 | V | *2 |
| Substrate voltage adjustment precision | Δ V _{SUB} | –3 | | +3 | % | |
| Reset gate clock voltage adjustment range | V _{RGL} | 0 | | 3.0 | V | *2 |
| Reset gate clock voltage adjustment precision | Δ V _{RGL} | –3 | | +3 | % | |
| Protective transistor bias | V _L | –11 | –10.5 | –10 | V | *3 |
| Horizontal register input source bias | V _{HIS} | 14.7 | 15.0 | 15.3 | V | V _{HIS} = V _{DD} |

Clock Voltage Conditions

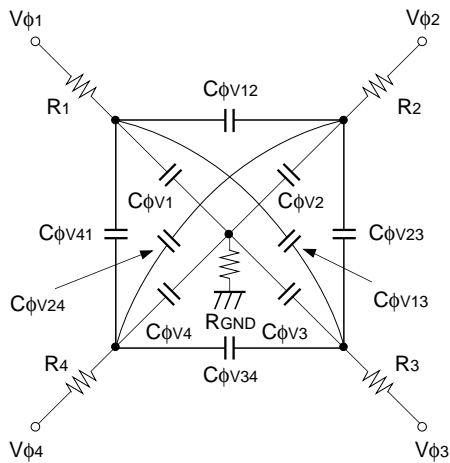
| Item | Symbol | Min. | Typ. | Max. | Unit | Waveform diagram | Remarks |
|-----------------------------------|--------------------------------------|------|------|------|------|------------------|--------------------------------------------------------|
| Readout clock voltage | V_{VT} | 14.5 | 15.0 | 15.5 | V | 1 | |
| Vertical transfer clock voltage | $V_{VH1}, V_{VH2}, V_{VH3}, V_{VH4}$ | -0.6 | | 0 | V | 2 | $V_{VH} = (V_{VH1} + V_{VH2})/2$ |
| | $V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}$ | | -9.6 | | V | 2 | $V_{VL} = (V_{VL3} + V_{VL4})/2$ |
| | $V_{\phi V}$ | 8.9 | | | V | 2 | $V_{\phi V} = V_{VHn} - V_{VLn} (n = 1 \text{ to } 4)$ |
| | $ V_{VH1} - V_{VH2} $ | | | 0.2 | V | 2 | |
| | $V_{VH3} - V_{VH}$ | -0.5 | | 0 | V | 2 | |
| | $V_{VH4} - V_{VH}$ | -0.5 | | 0 | V | 2 | |
| | V_{VHH} | | | 0.8 | V | 2 | High-level coupling |
| | V_{VHL} | | | 1.0 | V | 2 | High-level coupling |
| | V_{VLH} | | | 0.8 | V | 2 | Low-level coupling |
| | V_{VLL} | | | 0.8 | V | 2 | Low-level coupling |
| Horizontal transfer clock voltage | $V_{\phi H}$ | 6.0 | | 8.0 | V | 3 | |
| | V_{HL} | -3.5 | | -3.0 | V | 3 | |
| Reset gate clock voltage | $V_{\phi RG}$ | 6.0 | | 13.0 | V | 3 | *1 |
| | V_{RGL} | 0 | | 3.0 | V | 3 | |
| Substrate clock voltage | $V_{\phi SUB}$ | 27.0 | | 32.0 | V | 4 | |

*1 The reset gate clock voltage need not be adjusted when the reset gate clock is driven when the specifications are as given below. In this case, the reset gate clock voltage setting indicated on the back of the image sensor has not significance.

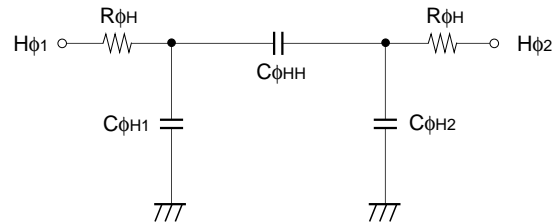
| Item | Symbol | Min. | Typ. | Max. | Unit | Waveform diagram | Remarks |
|--------------------------|---------------|------|------|------|------|------------------|---------|
| Reset gate clock voltage | V_{RGL} | -0.2 | 0 | 0.2 | V | 3 | |
| | $V_{\phi RG}$ | 8.5 | 9.0 | 9.5 | V | 3 | |

Clock Equivalent Circuit Constant

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|-------------------------------------------------------|------------------------------|------|------|------|----------|---------|
| Capacitance between vertical transfer clock and GND | $C_{\phi V1}, C_{\phi V3}$ | | 2700 | | pF | |
| | $C_{\phi V2}, C_{\phi V4}$ | | 2700 | | pF | |
| Capacitance between vertical transfer clocks | $C_{\phi V12}, C_{\phi V34}$ | | 2100 | | pF | |
| | $C_{\phi V23}, C_{\phi V41}$ | | 900 | | pF | |
| | $C_{\phi V13}$ | | 1000 | | pF | |
| | $C_{\phi V24}$ | | 500 | | pF | |
| Capacitance between horizontal transfer clock and GND | $C_{\phi H1}, C_{\phi H2}$ | | 47 | | pF | |
| Capacitance between horizontal transfer clocks | $C_{\phi HH}$ | | 58 | | pF | |
| Capacitance between reset gate clock and GND | $C_{\phi RG}$ | | 7 | | pF | |
| Capacitance between substrate clock and GND | $C_{\phi SUB}$ | | 800 | | pF | |
| Vertical transfer clock series resistor | R_1, R_2, R_3, R_4 | | 22 | | Ω | |
| Vertical transfer clock ground resistor | R_{GND} | | 3 | | Ω | |
| Horizontal transfer clock series resistor | $R_{\phi H}$ | | 10 | | Ω | |



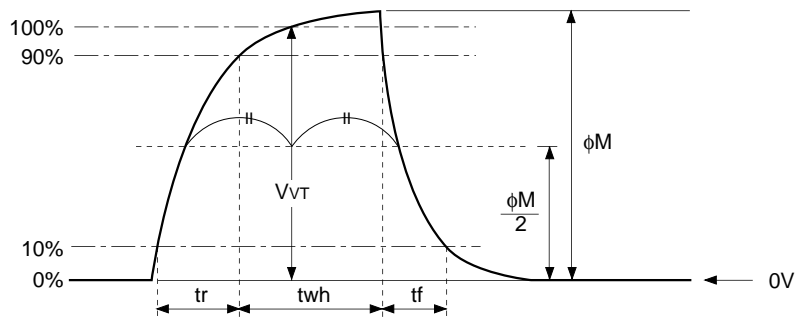
Vertical transfer clock equivalent circuit



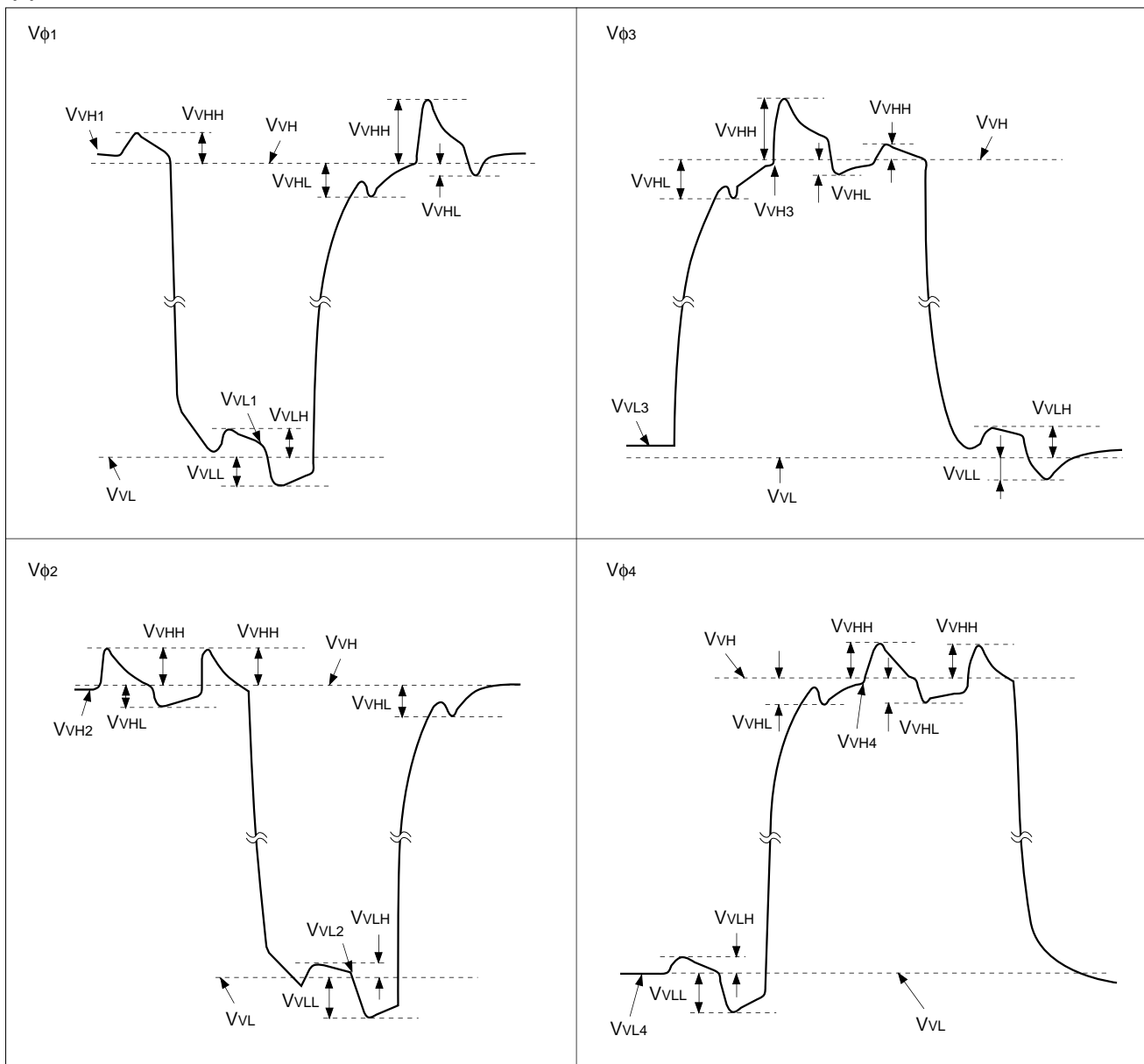
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

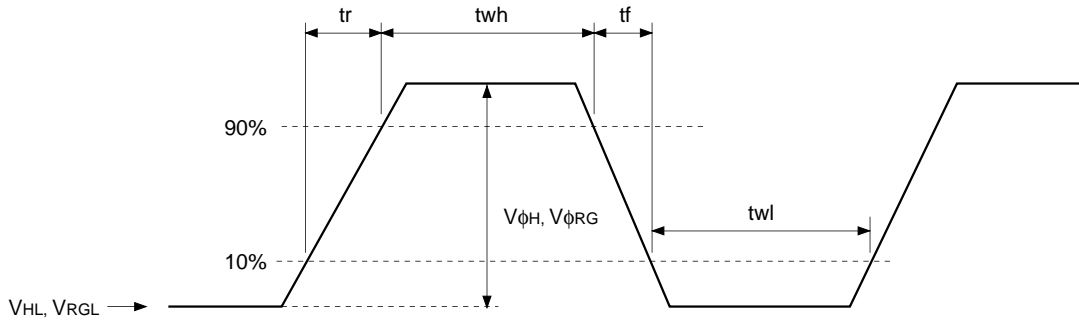


$$V_{VH} = (V_{VH1} + V_{VH2})/2$$

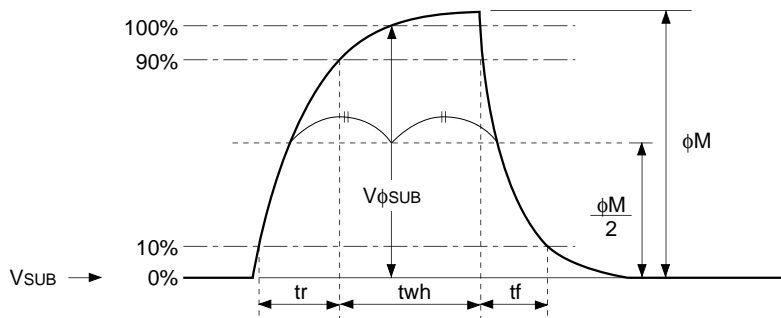
$$V_{VL} = (V_{VL3} + V_{VL4})/2$$

$$V_{\phi V} = V_{VHn} - V_{VLn} \quad (n = 1 \text{ to } 4)$$

(3) Horizontal transfer clock waveform - Reset gate clock waveform



(4) Substrate clock waveform



Clock Switching Characteristics

| Item | Symbol | twh | | | twl | | | tr | | | tf | | | Unit | Remarks |
|---------------------------|--------------------------|------|------|------|------|------|------|------|------|------|------|------|------|---------------|-----------------------------------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Readout clock | V_T | 2.3 | 2.5 | | | | | | 0.5 | | | 0.5 | | μs | During readout |
| Vertical transfer clock | $V_{\phi 1}, V_{\phi 2}$ | | 62.6 | | | 0.74 | | | 0.1 | | | 0.1 | | μs | During imaging |
| | $V_{\phi 3}, V_{\phi 4}$ | | 1.3 | | | 62.1 | | | 0.1 | | | 0.1 | | μs | |
| Horizontal transfer clock | H_{ϕ} | | 20 | | | 20 | | | 15 | 19 | | 15 | 19 | ns | During imaging |
| | $H_{\phi 1}$ | | 5.38 | | | | | | 0.01 | | | 0.01 | | μs | During parallel-serial conversion |
| | $H_{\phi 2}$ | | | | | 5.38 | | | 0.01 | | | 0.01 | | μs | |
| Reset gate clock | ϕ_{RG} | 11 | 13 | | | 51 | | | 2.0 | | | 2.0 | | ns | |
| Substrate clock | ϕ_{SUB} | 1.5 | 1.8 | | | | | | | | | 0.5 | | μs | During drain charge |

Image Sensor Characteristics

(Ta = 25°C)

| Item | Symbol | Min. | Typ. | Max. | Unit | Measurement method | Remarks |
|----------------------|--------|------|--------|--------|------|--------------------|-----------|
| Sensitivity | S | 500 | 700 | | mV | 1 | |
| Saturation signal | Vsat | 800 | | | mV | 2 | Ta = 60°C |
| Smear | Sm | | 0.0001 | 0.0003 | % | 3 | |
| Video signal shading | SH | | | 25 | % | 4 | |
| Dark signal | Vdt | | | 2 | mV | 5 | Ta = 60°C |
| Dark signal shading | ΔVdt | | | 1 | mV | 6 | Ta = 60°C |
| Flicker | F | | | 5 | % | 7 | |
| Lag | Lag | | | 0.5 | % | 8 | |

Image Sensor Characteristics Measurement Method

◎ Measurement conditions

- 1) In the following measurements, the substrate voltage and the reset gate clock voltage are set to the values indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.
- 2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, and the value measured at point [*A] in the drive circuit example is used.

◎ Definition of standard imaging conditions

1) Standard imaging condition I:

Use a pattern box (luminance 706cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.00mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity luminous intensity.

2) Standard imaging condition II :

Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.00mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity

Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (Vs) at the center of the screen and substitute the value into the following formula.

$$S = V_s \times \frac{250}{60} \text{ [mV]}$$

2. Saturation signal

Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with average value of signal output, 350mV, measure the minimum value of the signal output.

3. Smear

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of the signal output, 350mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value VSm [mV] of the signal output and substitute the value into the following formula.

$$S_m = \frac{V_{Sm}}{350} \times \frac{1}{500} \times \frac{1}{10} \times 100 [\%] \text{ (1/10V method conversion value)}$$

4. Video signal shading

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 350mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (V_{max} - V_{min})/350 \times 100 [\%]$$

5. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta V_{dt} = V_{dmax} - V_{dmin} [\text{mV}]$$

7. Flicker

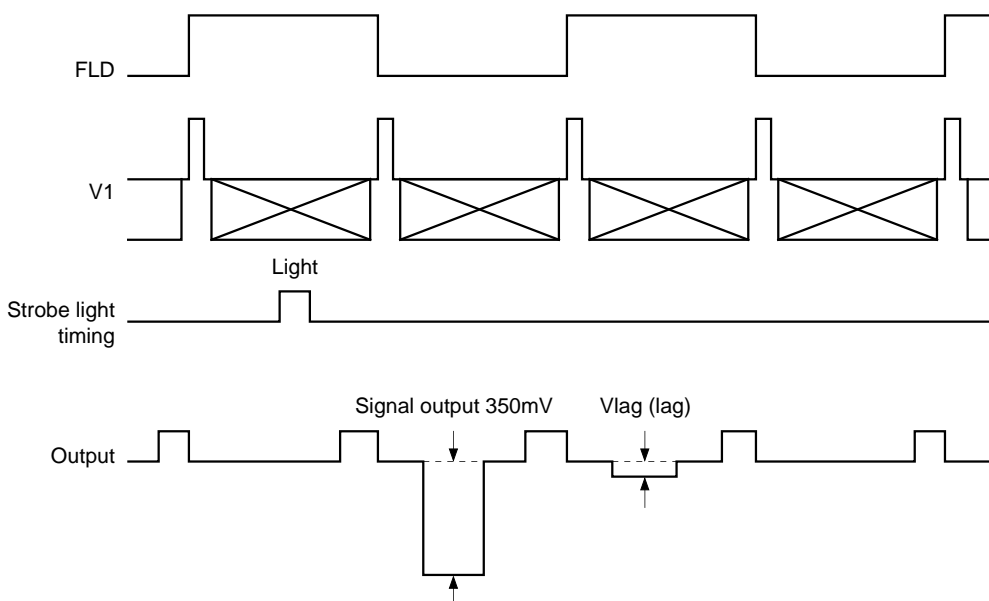
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the signal output is 350mV, and then measure the difference in the signal level between fields (ΔV_f [mV]). Then substitute the value into the following formula.

$$F = (\Delta V_f / 350) \times 100 [\%]$$

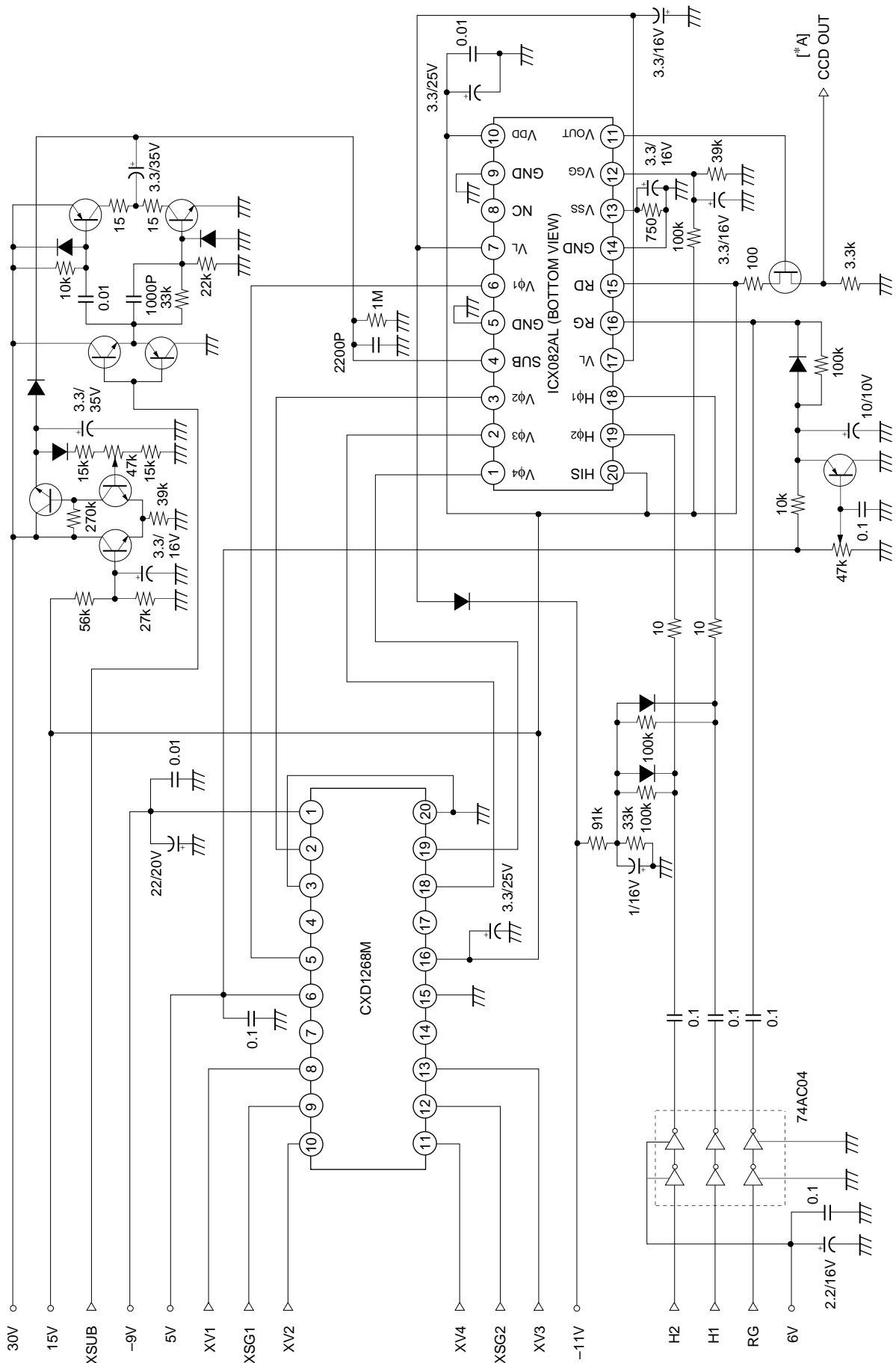
8. Lag

Adjust the signal output value generated by strobe light to 350mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

$$Lag = (V_{lag} / 350) \times 100 [\%]$$

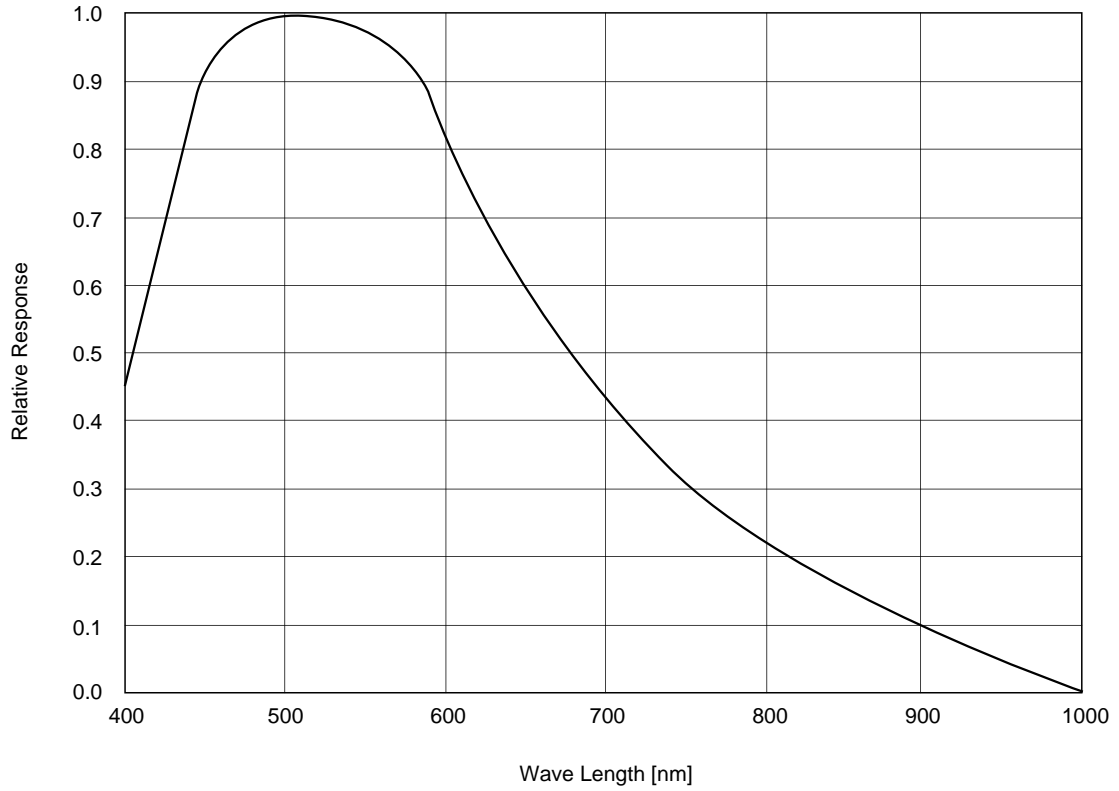


Drive Circuit

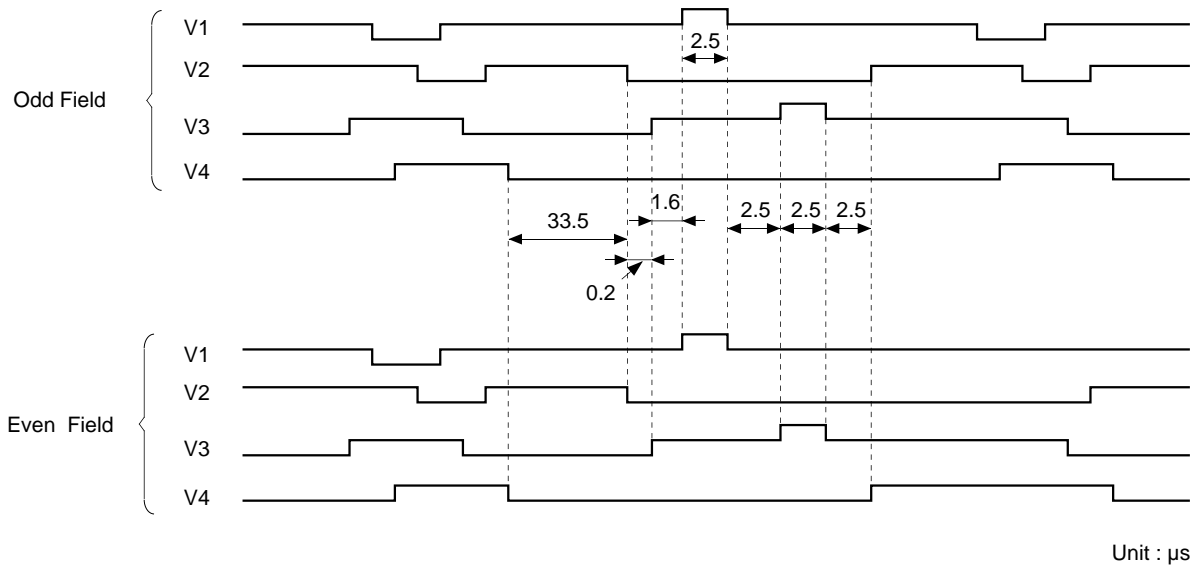


Spectral Sensitivity Characteristics

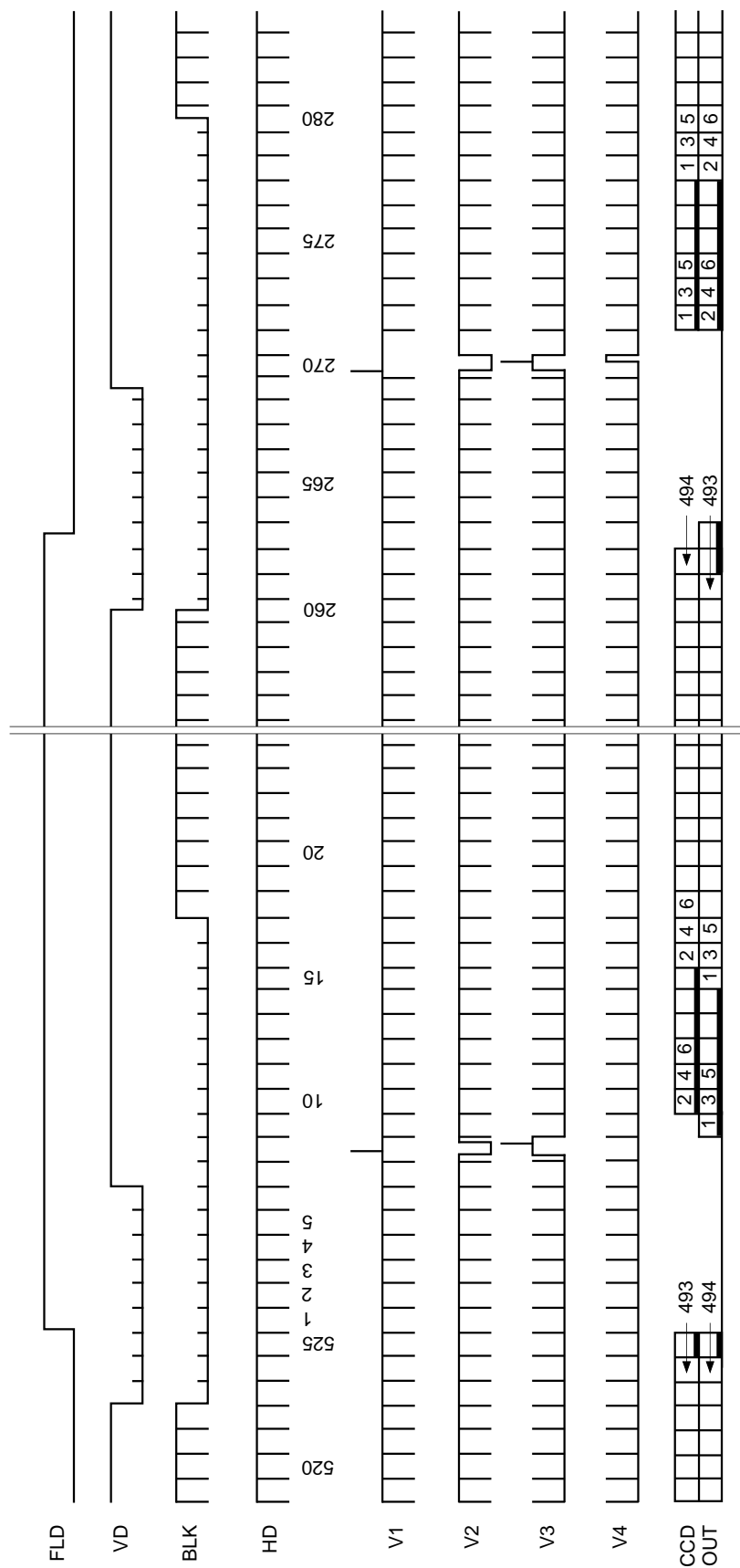
(includes lens characteristics, excludes light source characteristics)



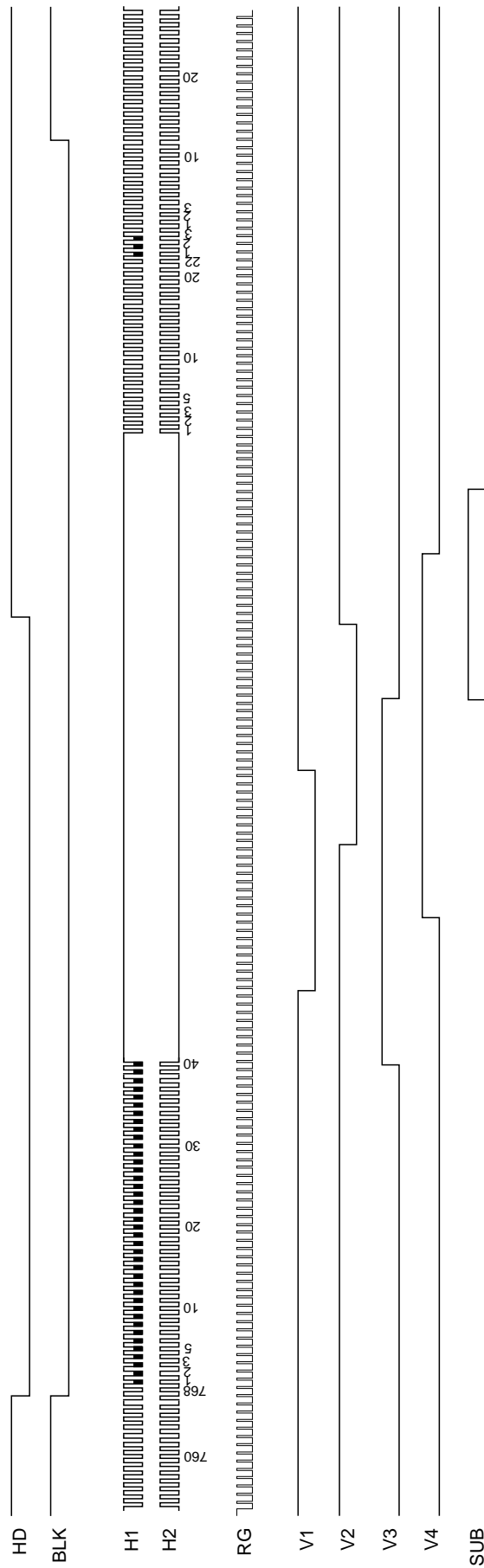
Sensor Readout Clock Timing Chart



Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

- a) Operate in clean environments (around class 1000 is appropriate).
 - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces.
Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
 - c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
 - d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
 - e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.
- 4) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.
- 5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- 6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

